REMARKS

In view of the foregoing amendments and the following remarks, reconsideration and allowance of this application is requested. Claims 1–23 remain pending in the application with Claims 1, 9, and 12 being independent.

Claims 1–18 and 21–22 are rejected under 35 U.S.C. 103(a) as being unpatentable over DeLuca et al (US Patent No 5,612,682) in view of Seo et al (US Patent No 5,063,597), Tran (US Patent No. 5,734,729), and Nagata (US Patent No. 6,114,981). The Applicant respectfully traverses these rejections.

The Examiner also rejects Claims 19–20 under 35 U.S.C. 103(a) as being unpatentable over DeLuca, Seo, Tran, and Nagata as applied to Claim 12, and further in view of Lipovski (US Patent No 6,675,002). The Applicant respectfully traverses these rejections.

The Examiner also rejects Claim 23 under 35 U.S.C. 103(a) as being unpatentable over DeLuca, Seo, Tran, and Nagata as applied to Claim 12 above, and further in view of Elliot (US PG Pub 2002/0077177). The Applicant respectfully traverses these rejections.

Regarding Claim 1 & 12, the Applicant requests reconsideration and withdrawal of the rejections for at least the reason that Seo teaches away from combining the references cited above. MPEP § 2145(D) states that, "It is improper to combine references where the references teach away from their combination." In Claim 1, the Applicant claims, "... a digital signal processor operable to... generate a disable signal; ...; and a digital-to-analog converter... having an input operable to receive the disable signal, the digital-to-analog converter muting the output... in response to the disable signal...". In Claim 12, the Applicant claims a method comprising, "... generating a disable signal; ...; generating an analog signal...; transmitting the disable signal to the digital-to-analog converter; and muting the analog signal in response to the transmitted disable signal."

Seo does not teach an analog-to-digital converter configured to receive a disable signal. Seo teaches a first switching circuit that receives a mute control and a first digital data from a DSP and a fourth digital data from a multiplier. The first switching circuit then selects and outputs selectively the first or the fourth digital data to a digital-to-analog converter (Seo, Column 3, Lines 32-38). The Applicant respectfully submits that the Examiner mistakenly states that the digital-to-analog converter receives the disable signal and mutes the output of the corresponding analog data in response thereto. It is the first switching circuit that receives the mute signal, not the digital-to-analog converter. Seo specifically teaches not to output the disable or mute signal to a digital-to-analog converter. Therefore, Seo teaches away from what the Applicant claims as the invention and away from combining the references as was suggested by the Examiner.

The Examiner has failed to show that Claims 1 & 12 are obvious in view of the references, and therefore, Claims 1 & 12 are patentable over the references. The Applicant respectfully requests reconsideration and withdrawal of the rejection for at least the reasons stated above.

Claims 2–8 and 13–23 depend either from independent Claim 1 or from independent Claim 12. Accordingly, the Applicant requests reconsideration and withdrawal of the rejections for Claims 2–8 and 13–23 for at least the reasons discussed above with respect to Claims 1 & 12.

Regarding Claim 9, the Applicant again requests reconsideration and withdrawal of the rejections for at least the reason that Seo teaches away from combining the references cited above. MPEP § 2145(D) states that, "It is improper to combine references where the references teach away from their combination." In Claim 9, the Applicant claims, "... a digital signal processor operable to... generate a disable signal, ..., and an analog amplifier... having an input operable to receive the disable signal, the amplifier muting the amplified output in response to the disable signal...".

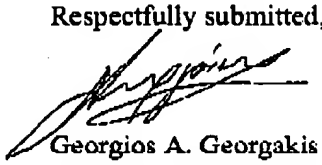
Seo does not teach an analog amplifier configured to receive a disable signal. Seo teaches a first switching circuit that receives a mute control and a first digital data from a DSP and a fourth digital data from a multiplier. The first switching circuit then selects and outputs selectively the first or the fourth digital data to a digital-to-analog converter (Seo, Column 3, Lines 32-38). It is the first switching circuit that receives the mute signal, not an analog amplifier. Seo specifically teaches not to output the disable or mute signal to an analog amplifier. Therefore, Seo teaches away from what the Applicant claims as the invention and away from combining the references as was suggested by the Examiner.

The Examiner has failed to show that Claim 9 is obvious in view of the references, and therefore, Claim 9 is patentable over the references. The Applicant respectfully requests reconsideration and withdrawal of the rejection for at least the reasons stated above.

Claims 10 & 11 depend from independent Claim 9. Accordingly, the Applicant requests reconsideration and withdrawal of the rejections for Claims 10 & 11 for at least the reasons discussed above with respect to Claim 9.

In view of these remarks and amendments, Applicant submits that this application is in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



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